REMARKS

This application has been reviewed in light of the Office Action dated July 22, 2002. Claims 1, 7, 9-11, 13-17, 21, and 23 are pending in this application. Claims 7, 9, 10, and 13-16 have been amended to have these claims depend from Claim 2, and Claims 11 and 17 have been amended to have these claims depend from Claim 1. Applicants submit that the changes to these claims do not, in any way, narrow the scope of these claims. Claims 1 and 21 are in independent form. Favorable reconsideration is requested.

First, Applicants gratefully acknowledge the indication that Claims 2, 3, 5, 7, 9, 10, 13-16, 22, 25, and 26 include allowable subject matter and would be allowable if rewritten in proper independent form. Claims 2, 3, 5, 7, 9, 10, 13-16, 22, 25, and 26 have not been so rewritten at this time because Applicants traverse the rejection of independent Claims 1 and 21, as described below.

The Office Action objected to the specification, asserting that reference numeral "1441" be changed to "441." Applicants have amended the specification, believe that the objection has been remedied, and respectfully request its withdrawal.

The Office Action objected to the drawings, asserting that reference numeral "30" in Figure 2 be changed to reference numeral --305--. Applicants enclose hereto a Letter Transmitting Corrected Drawing, which amends Figure 2 accordingly. Applicants believe that the objection has been remedied and respectfully request its withdrawal.

The Office Action objected to Claim 12, asserting that "vinary" at line 12 be changed to --binary--. Applicants have amended Claim 12 accordingly, believe the objection has been remedied, and respectfully request withdrawal of the objection.

The Office Action rejected Claims 1, 11, 12, 17, 20, 21, 23, 24, and 28-30 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,318,828 B1 (Barbour et

al.). Applicants respectfully traverse this rejection.

Applicants enclose hereto sworn translations of Japanese applications 10-306179 and 10-306182, both of which were filed October 27, 1998, from which the present application claims priority. Applicants note that Barbour et al. has an effective date of February 19, 1999, which is later than the filing date of October 27, 1998 for Japanese applications 10-306179 and 10-306182. Thus, Applicants submit that Barbour et al. is not prior art and therefore respectfully request withdrawal of this rejection based on Barbour et al.

Applicants also enclose hereto a copy of the IDS submitted on April 10, 2001, as requested by the Examiner at page 6 of the Office Action.

Applicants' undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

Peter C. Thales

Attorney for Applicants

Registration No. 47,138

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200

NY_MAIN 309479 v 1

VERSION WITH MARKINGS SHOWING CHANGES
MADE TO SPECIFICATION (as of 11/22/02)

The paragraph at page 23, line 10 has been amended as follows:

Also in the foregoing embodiment, the ink jet printer 300 causes the fuse logic circuit 442 to only execute the readout of the data stored in the fuse RPM [1441] 441, but it is also possible to execute the data writing or to selectively execute the data readout and the data writing.

NY_MAIN 309510 v 1

C

VERSION WITH MARKINGS SHOWING CHANGES
MADE TO CLAIMS (as of 11/22/02)

1. (Amended) A head substrate of a printing head detachably mounted on a printer main body, comprising:

plural external connection terminals individually receiving, from the exterior, a binary logic signal corresponding to whether or not to execute a recording operation, a recording image signal and a clock signal;

recording execution means for executing the recording operation according to the recording image signal and the clock signal entered through said external connection terminals, in case said binary logic signal is in a first state;

data memory means for executing a memory access which is at least either of data writing and data readout; and

memory access means for recognizing said binary logic signal as an access permission signal and executing the memory access to said data memory means at a timing [corresponding to the clock signal] when said logic signal is in a second state.

7. (Twice Amended) A head substrate according to [claims 2 or 3] <u>claim 2</u>, wherein:

said recording execution means includes a shift register which is reset by a reset signal externally entered into one of said external connection terminals and is adapted to temporarily hold and parallel output, at a timing corresponding to the clock signal, the recording

image signal serially entered into another of said external connection terminals; and

said common terminal wiring means is adapted for supplying said memory access means with the reset signal for said shift register, as said binary logic signal constituting said access permission signal.

9. (Twice Amended) A head substrate according to [claims 2 or 3] claim 2, wherein:

said recording execution means includes a shift register which is adapted to be reset by a reset signal externally entered into one of said external connection terminals and then to temporarily hold and parallel output, at a timing corresponding to the clock signal, the recording image signal serially entered into another of said external connection terminals, and a latch circuit which is adapted to be reset by said reset signal and then to temporarily hold and output the recording image signal parallel outputted from said shift register; and

said common terminal wiring means is adapted for supplying said memory access means with said reset signal as said binary logic signal constituting said access permission signal.

10. (Twice Amended) A head substrate according to [claims 2 or 3] claim 2, wherein:

said recording execution means includes a shift register which is adapted to be reset by a reset signal externally entered into one of said external connection terminals and then to temporarily hold and parallel output, at a timing corresponding to the clock signal, the

recording image signal serially entered into another of said external connection terminals, and a latch circuit which is adapted to temporarily hold and output the recording image signal parallel outputted from said shift register at a timing corresponding to a latch signal externally entered into still another of said external connection terminals; and

said common terminal wiring means is adapted for supplying said memory access means with said latch signal as said binary logic signal constituting said access permission signal.

11. (Twice Amended) A head substrate according to [any of claims 1, 2, 3, and 5] claim 1, wherein said recording execution means includes plural recording elements for recording the recording image signal parallel outputted from said latch circuit, corresponding to a recording pulse signal externally entered into one of said external connection terminals.

13. (Twice Amended) A head substrate according to [any of claims 2, 3, and 5] claim 2, wherein said common terminal wiring means is adapted to supply said memory access means with the clock signal for said recording image signal, as a memory clock signal.

14. (Twice Amended) A head substrate according to [any of claims 2, 3, and 5] claim 2, wherein:

said data memory means is means for executing both data writing and data readout as the memory access;

said memory access means is means for selectively executing either of data writing into and data readout from said data memory means corresponding to an externally entered mode switching signal; and

said common terminal wiring means is adapted for supplying said memory access means with the input signal to one of said external connection terminals as the mode switching signal.

15. (Twice Amended) A head substrate according to [any of claims 2, 3, and 5] claim 2, wherein:

said recording execution means is adapted for receiving a driving electric power externally entered from one of said external connection terminals; and

said common terminal wiring means is adapted for supplying said memory access means with the driving electric power for said recording execution means.

16. (Twice Amended) A head substrate according to [any of claims 2, 3, and 5] claim 2, wherein said external connection terminals, said recording execution means, said data memory means, said memory access means and said common terminal wiring means are constituted by films formed on one base substrate.

17. (Twice Amended) A printing head detachably mounted on a printer main body, comprising a head substrate according to [any of claims 1, 2, 3, and 5] claim 1.

21. (Amended) A printing head detachably mounted on a printer main body, comprising:

plural external connection terminals individually receiving, from the exterior, a binary logic signal corresponding to whether or not to execute a recording operation, a recording image signal and a clock signal;

recording execution means for executing the recording operation according to the recording image signal and the clock signal entered through said external connection terminals, in case said binary logic signal is in a first state;

data memory means for executing a memory access which is at least either of data writing and data readout; and

memory access means for recognizing said binary logical signal as an access permission signal and executing the memory access to said data memory means at a timing [corresponding to the clock signal] when said logical signal in a second state.

23. (Amended) A printing apparatus comprising:

a printing head according to claim 17;

input means for individually transmitting the binary logic signal of the first state and various signals such as the recording image signal and the clock signal respectively to plurality of said external connection terminals of said printing head, thereby causing said recording execution means to execute a recording operation; and

access control means for transmitting the [vinary] <u>binary</u> logic signal of

the second state and the clock signal, etc. to said plural external connection terminals of said printing head, thereby causing said memory access means to execute the memory access.